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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,254	10/30/2003	Ravid Guy	206,322	2540

38137 7590 11/20/2007
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EXAMINER	
PATEL, CHANDRAHAS B	
ART UNIT	**PAPER NUMBER**
2616	

MAIL DATE	DELIVERY MODE
11/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/699,254	GUY ET AL.	
	Examiner	Art Unit	
	Chandrahas Patel	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 9/12/2007 have been fully considered but they are not persuasive.

Examiner withdraws rejection to claims 2, 3, 11, 12, 21, 23 under 35 U.S.C. 112 in light of submitted amendments.

Regarding claims 1, 10 and 20, applicant states that both configuration port and data input ports are coupled to the PHY device. Fig. 1 of Fallside teaches FPGA 104 is connected to data input port via connection from PHY 102 to FPGA 104 that receives communication data from the communication channel. Configuration port which can be same as data input port is also connected to FPGA 104 from PHY 102. Fig. 2, step 156 states receiving configuration data from a communication channel which is used to reconfigure FPGA 104. Applicant states that only a single port is coupled to the PHY. Examiner agrees that only a single port is connected to the PHY. However, the claim does not state that a configuration port and a data input port are separate ports. Therefore, the same port can be used to reconfigure the FPGA 104 and also communicate data over the network. The storage element is used to store the configuration file that could be used to program FPGA 104 and does not teach away from the invention.

Regarding claims 2, 11 and 21, applicant states that the network node comprises no non-volatile memory. Examiner agrees with this. However, RAM is volatile memory since RAM requires power to maintain the stored information (See Page 437 of Microsoft Computer Dictionary, Fifth Edition, ISBN 0-7356-1495-4). The claim feature requires no non-volatile

memory. Fallside's network node does not have non-volatile memory. It has volatile memory as mentioned above.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-4, 6-8, 10-17, 20-24, 26-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Fallside et al. (USPN 6,326,806).

Regarding claim 1, Fallside teaches network node apparatus **[Fig. 1, 100]**, comprising: a physical layer interface (PHY) device **[Fig. 1, 102]**, which comprises a network port and a data output port, and is adapted to receive signals from a communication network through the network port **[Fig. 1, 102, receives communication from communication channel]** and to process the signals in accordance with a predetermined physical layer protocol so as to generate a digital data output at the data output port **[Col. 3, lines 26-29]**; and a field-programmable logic device **[Fig. 1, 104]**, comprising: a configuration port, which is coupled to the data output port of the PHY device so as to receive program code, which is transmitted over the network during a programming phase in order to program the field-programmable logic device **[Fig. 1, 104 receives data from PHY device, Col. 4, lines 14-18]**; and a data input port, which is also coupled to the data output port of the PHY device so as to receive communication data transmitted over the network following conclusion of the programming phase, whereupon the field programmable logic device is programmed by the program code to process the communication data in accordance with a predetermined data link layer protocol **[FPGA 104**

receives bit stream from PHY 102 from communication channel which is also used for communication, Col. 5, lines 40-63].

Regarding claims 2, 11, 21, Fallside teaches the apparatus comprises volatile memory for holding the program code **[Fig. 3, 208, Col. 9, lines 8-11]**.

Regarding claims 3, 12, Fallside teaches the configuration port and data input ports are connected in parallel to the data port without substantially other logic components intervening between the ports **[Fig. 1, 102 is connected to 106 in parallel with just one logical component, also see Col. 3, lines 36-38]**.

Regarding claims 4, 13, 24, Fallside teaches the physical layer protocol and data link layer protocol comprises Ethernet protocols **[Col. 4, lines 42-44]**.

Regarding claim 6, Fallside teaches during the programming phase, the digital data output comprises a sequence of clock bits, which are generated by the PHY device responsively to the signals received from the communication network **[Col. 8, lines 19-23]**, and wherein the field programmable logic device comprises a clock input, which is coupled to receive the clock bits so as to clock the program code into the input port **[Col. 6, lines 30-31]**.

Regarding claims 7 and 16, Fallside teaches field programmable logic device further comprises a data transmit port and is further programmed by the program code to generate data frames at the data transmit port in accordance with the data link protocol **[Col. 3, lines 29-34, where TCP/IP stack can be implemented in FPGA]**, and wherein the PHY device comprises a data receive port, which is coupled to the data transmit port so as to receive the data frames generated by the field programmable logic device for transmission over the communication

network via the network port **[Fig. 1, 102 receives data from 104 for transmission to communication channel]**.

Regarding claims 8, 17, and 29, Fallside teaches the field programmable logic device comprises a field programmable gate array **[Fig. 1, 104]**.

Regarding claim 10, Fallside teaches apparatus for communication over a network **[Fig. 1, 100]**, which operates in accordance with a predetermined physical layer protocol **[Col. 4, lines 42-44]**, the apparatus comprising: a code server, which is adapted to transmit program code over the network during a programming phase of the apparatus **[Col. 5, lines 28-39]**; and a network node **[Fig. 1, 100]**, comprising: a physical layer interface (PHY) device **[Fig. 1, 102]**, which comprises a network port and a data output port, and is adapted to receive signals from the network through the network port **[Fig. 1, 102, receives communication from communication channel]** and to process the signals in accordance with the physical layer protocol so as to generate a digital data output at the data output port **[Col. 3, lines 26-29]**; and a field-programmable logic device **[Fig. 1, 104]**, comprising: a configuration port, which is coupled to the data output port of the PHY device so as to receive the program code transmitted by the code server in order to program the field-programmable logic device **[Fig. 1, 104 receives data from PHY device, Col. 4, lines 14-18]**; and comprising a data input port, which is also coupled to the data output port of the PHY device so as to receive communication data transmitted over the network following conclusion of the programming phase, whereupon the field programmable logic device is programmed by the program code to process the communication data in accordance with a predetermined data link layer protocol **[FPGA 104 receives bit stream from**

PHY 102 from communication channel which is also used for communication, Col. 5, lines 40-63].

Regarding claims 14 and 26, Fallside teaches the code server is adapted to frame the program code in data frames in accordance with the physical layer protocol, so as to cause the PHY device to output the program code through the data output port in a format suitable for programming the field programmable logic device **[Col. 4, lines 6-11]**.

Regarding claims 15 and 27, Fallside teaches the code server is adapted to incorporate in the data frames, together with the program code, a sequence of clock bits **[Col. 8, lines 19-25]**, and wherein the field programmable logic device comprises a clock input, which is coupled to receive the clock bits from the PHY device so as to clock the program code into the configuration port **[Col. 6, lines 30-31]**.

Regarding claim 20, Fallside teaches a method for network communication **[Abstract]**, comprising: coupling a node, which comprises a programmable processor and a physical layer interface (PHY) device, to receive signals from a communication network via a network port of the PHY device **[Fig. 1, 102, 104, PHY 102 receives communication data from communication channel]**; processing the signals at the node in accordance with a predetermined physical layer protocol so as to generate a digital data output at a data output port of the PHY device **[Col. 3, lines 26-29]**; transmitting the signals on the network in accordance with the physical layer protocol during a programming phase of the network so as to convey program code to the node **[Fig. 1, 104 receives data from PHY device, Col. 3, lines 26-29]**; coupling the data output port of the PHY device to a configuration port of the programmable processor, so as to program the processor using the transmitted program code **[Fig. 1, 104 receives data from**

PHY device, Col. 4, lines 14-18]; following conclusion of the programming phase, transmitting the signals on the network in accordance with the physical layer protocol and with a predetermined data link layer protocol so as to convey communication data over the network to the node **[FPGA 104 uses PHY 102 communication channel which is used for communication, Col. 5, lines 40-63]**; and coupling the data output port of the PHY device to a data input port of the programmable processor, so that following the conclusion of the programming phase, the processor processes the communication data, responsively to the program code, in accordance with the data link layer protocol **[Coupling Fig. 1, 104 to 102, Col. 5, lines 40-63]**.

Regarding claim 22, Fallside teaches coupling the digital data output to the configuration port comprises connecting the configuration port and the data input port in parallel to receive the digital data output **[Fig. 1, 102 is connected to 106 in parallel]**.

Regarding claim 23, Fallside teaches connecting the configuration port and the data input port in parallel comprises connecting the configuration port and the data input port substantially without other logic components intervening between the ports **[Fig. 1, 102 is connected to 106 in parallel with just one logical component, also see Col. 3, lines 36-38]**.

Regarding claim 28, Fallside teaches the program code further causes the programmable processor to generate data frames in accordance with the data link protocol for transmission over the communication network **[Col. 3, lines 29-34, where TCP/IP stack can be implemented in FPGA]**.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 5 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fallside et al. (USPN 6,326,806, Herein as Fallside) in view of Magal et al. (USPN 6,933,745, Herein as Magal).

Regarding claims 5 and 25, Fallside teaches the apparatus and the method as discussed in rejection of claims 4 and 24 respectively.

However, Fallside does not teach the PHY device is adapted to generate the digital data output in accordance with an Ethernet media independent interface (MII).

Magal teaches the PHY device can generate the digital data output in accordance with an Ethernet media independent interface (MII) **[Abstract]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Ethernet media independent interface (MII) since it's a well-known standard interface specified in IEEE 802.3 standards **[Col. 1, lines 14-18]**.

6. Claims 9, 18, 19, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fallside et al. (USPN 6,326,806, Herein as Fallside) in view of Mantey et al. (USPN 6,918,027, Herein as Mantey).

Regarding claims 9, 18, Fallside teaches the apparatus as discussed in rejection of claims 1, 10.

However, Fallside does not teach the apparatus has an identification component holding an identification value and coupled to be read by the field programmable logic device, so that when the field programmable logic device is programmed by the program code, the field programmable logic device conveys the identification value over the network to a code server.

Mantey teaches the apparatus has an identification component holding an identification value and coupled to be read by the field programmable logic device, so that when the field programmable logic device is programmed by the program code, the field programmable logic device conveys the identification value over the network to a code server **[Col. 8, lines 9-19]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have an ID value so that appropriate FPGA code could be located in a database **[Col. 8, lines 13-19]**.

Regarding claim 19, Fallside teaches the program code comprises start-up program code and operation program code, wherein code server is adapted to initially transmit the start-up program code to the network node **[Col. 3, lines 36-38]**.

However, Fallside does not teach that the network node conveys the identification value over the network to the code server, and wherein the code server is further adapted, upon receiving the identification value, to select the operational program code to transmit to the network node responsively to the identification value.

Mantey teaches the network node conveys the identification value over the network to the code server, and wherein the code server is further adapted, upon receiving the identification value, to select the operational program code to transmit to the network node responsively to the identification value **[Col. 8, lines 9-19]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the identification value so that appropriate FPGA code could be located in a database **[Col. 8, lines 13-19]**.

Regarding claim 30, Fallside teaches initially transmitting start-up program code to the network node **[Col. 3, lines 36-38]**, and the program code is in accordance with the data link layer protocol **[Col. 3, lines 26-31]**.

However, Fallside does not teach the node comprises an identification (ID) component holding an identification value and coupled to be read by the programmable processor, and wherein transmitting the signals during the programming phase comprises: the programmable processor to conveys the identification value over the network to the code server; receiving the identification value from the node; and selecting operational program code to transmit to the node, responsively to the identification value, so as to cause the processor to processes the communication data, responsively to the operational program code.

Mantey teaches the node comprises an identification (ID) component holding an identification value and coupled to be read by the programmable processor, and wherein transmitting the signals during the programming phase comprises: the programmable processor to conveys the identification value over the network to the code server; receiving the identification value from the node; and selecting operational program code to transmit to the node, responsively to the identification value, so as to cause the processor to processes the communication data, responsively to the operational program code **[Col. 8, lines 9-19]**.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the identification value so that appropriate FPGA code could be located in a database **[Col. 8, lines 13-19]**.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chandrahas Patel whose telephone number is 571-270-1211. The examiner can normally be reached on Monday through Thursday 7:30 to 17:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CBP

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER